FPGA Based Time-of-Flight 3D Camera Characterization System

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Abstract—In this paper we present an FPGA based characterization system for our 3D TOF distance sensors supporting up to 128 × 128 pixels. The system is capable of flexibly generating all control signals required for a typical TOF measurement. Their properties can be changed within a very broad range. The cycle-to-cycle jitter of those signals was reduced to 1 ps by ECL circuitry. This is equivalent to a standard deviation of the measured distance of 0.15 mm. Furthermore, the system is able to preprocess the distance information before transferring the data to a terminal PC, which reduces the data load on the USB interface. The system includes an averaging function with a maximum of 256 elements to reduce the standard deviation of precision distance measurement sensors. A novel fiber based setup is introduced to systemize the characterization process. By means of averaging a standard deviation of 2 mm could be achieved with one of our 3D TOF distance sensors.

Keywords—characterization system, FPGA, optical distance sensor, TOF sensor, 3D camera, time-of-flight

I. INTRODUCTION

In recent years great improvements were made in the field of optical distance measurement. As this method does not require any contact to an object, it led to vast interest from industrial as well as entertainment product manufacturers. For instance Microsoft introduced Kinect for its XBox console and ASUS presented a range sensor called Xtion. Both systems are based on technology from Primesense [1]. By means of a laser an infrared grid is projected on the objects in front of the range sensor. This grid is deformed according to the shape and the distance of the objects. By recording the deformation of the grid with an ordinary 2D camera, the distance information can be extracted. The major advantage of this system is its low cost. Only off-the-shelf components are required. However, these range sensors are very prone to background light.

Another approach to optically measure a distance is by means of the time-of-flight (TOF) method. Here an optical signal is sent to an object, where it is backscattered and then received by a TOF sensor. Because the signal is delayed by the finite speed of light \( c \), the distance can be calculated from the phase difference \( \varphi_{\text{TOF}} \) of the sent and the received optical wave. Some range measurement techniques based on the TOF-method proved to be very insensitive to background light [2]. This makes the TOF distance measurement method interesting for automotive and industrial applications.

In this paper we present a system for characterizing TOF-camera chips. The system is capable of the following tasks:

- Flexible generation of all control signals and variation of their properties in a broad range to characterize the TOF chips
- Read-in of the analogous output voltages of the TOF chip generated during a measurement cycle
- Pre-processing of one distance data frame independent of a terminal PC
- Transmission of the data to a terminal PC
- Ability to quickly implement further signal-processing based features within the VHDL code

All relevant parameters like the shape of control signal waveforms, the pixel array size or other pre-processing constraints are resizeable on-the-fly to ease the characterization of a TOF camera chip. The system is capable of various pixel array sizes of the camera up to a maximum of 128 × 128 pixels.

II. TOF WORKING PRINCIPLE

Basically a TOF distance measurement takes advantage of
the finite speed of light \( c_0 \). To acquire the desired distance information an optical signal is sent from the sensor, illustrated amongst others in Fig. 1, to an object in front of the camera. There a fraction of the signal is backscattered towards the camera. Once the optical signal is received it is correlated with the sent one resulting in a correlation triangle similar to that in Fig. 2. The angular phase shift \( \phi_{\text{ToF}} \) of the correlation triangle is equivalent to the phase shift between the sent and received signal. By determining \( \phi_{\text{ToF}} \) of the correlation triangle the propagation time of the optical signal can be calculated. Subsequently the distance of the object can be acquired by (1).

\[
d_{\text{obj}} = \frac{\phi_{\text{ToF}} c_0}{2\pi f_{\text{mod}}} \tag{1}
\]

When starting a measurement cycle a continuous modulation clock is generated by the control logic block, illustrated amongst others in Fig. 1. This signal is emitted by an illumination source. At an object at the distance \( d_{\text{obj}} \) a fraction of the signal is backscattered to a TOF measurement pixel. When the light signal is received at the pixel it was delayed proportional to the finite speed of light \( c_0 \) and the distance of the object \( d_{\text{obj}} \). Meanwhile a second clock, the reference clock is transmitted electrically onboard to the TOF pixel. It has the very same frequency as the modulation clock. The phase delay \( \phi \) of the modulation clock to the reference clock can be varied in dedicated steps to correlate both signals. To acquire one point of the correlation triangle a certain phase shift \( \phi = \phi_2 \) is applied to the modulation clock. Then the pixel integrates both the optical modulation and the electrical reference clock during the integration time according to the correlation operation. After the integration process is completed the correlation voltage \( V_{\text{corr}} \) can be read from the sensor pixel. Then a new measurement with a phase \( \phi = \phi_2 \) of the reference clock can be started.

By successively varying \( \phi \) in dedicated steps from 0 to \( 2\pi \) a correlation triangle similar to the one depicted in Fig. 2 can be generated. The phase shift \( \phi_{\text{ToF}} \) of the optical modulation signal is proportional to the time it travels over the distance \( d_{\text{obj}} \) due to \( c_0 \).

To acquire the distance information from the correlation triangle, it is Fourier transformed with a Fast Fourier Transform (FFT) algorithm. \( \phi_{\text{ToF}} \) can finally be obtained from the fundamental wave of the correlation triangle depicted in Fig. 2 resulting from the FFT operation. This task has to be performed for every single pixel, resulting in a 3D image of the space in front of the camera. Moreover, the higher harmonics obtained by the FFT can be used for further analytics of the TOF measurement. For instance a TOF range sensor shows a certain dependence of the measured distance on the electrical bandwidth of the illumination source [3]. This effect can be corrected by, e.g., a reference path [3] or by acquiring the higher harmonics of the triangle [4].

### III. MEASUREMENT SYSTEM IN DETAIL

The TOF measurement setup, using an FPGA, is illustrated in Fig. 3. Via a USB interface a terminal PC directs the Stratix IV FPGA to start a new measurement. The device generates the appropriate control signals and sends them to the camera chip and the illumination source, respectively. In our measurement setup typically a laser is used. Lasers possess a large signal bandwidth making them ideal for characterizing TOF pixels. The light is coupled into the pixel by means of an optical fiber, thus removing optical components such as lenses as possible error sources. Another advantage of a fiber based setup is that the received optical power of the TOF pixel can be precisely adjusted. Alternatively, a LED light source can be connected instead of the laser. In this case no fiber is necessary to guide the modulated light to the TOF pixels. After the measurement is completed the FPGA reads in the output signals from the camera chip, pre-processes the data internally and sends the data to the terminal PC. Additionally, the PC can change the laser power via a second USB connection.

The pixels of the TOF camera used in this measurement system are described in, e.g., [5]. They are able to suppress very high background light intensities. To use this feature a CALIB pin has to be set before every single measurement. When this is done, the strength of the background light is sensed and stored within a section of the pixel. This postpones a possible saturation of the correlation circuitry of the pixel during integration. After the background light calibration is completed, the old integration charge stored within the integration capacitor of every pixel is dumped by setting the RESET pin. This pin is set for an adjustable amount of time. Then the pixel is ready to perform the actual measurement process. As described above the integration time is started by generating both the reference and the modulation clock with a dedicated phase shift \( \phi \). Furthermore, those signals are fed to the pixel and the illumination source, respectively. By finishing the integration time, one phase step of the correlation triangle from every single pixel of the camera was acquired. The FPGA directs the camera chip to issue the obtained voltages to the output. The voltages are then converted by an ADC and are stored to a memory. This whole process is performed for \( N \) phase steps to obtain a complete correlation triangle. Every correlation voltage for each pixel is stored to the SRAM-blocks of the FPGA. After a complete correlation triangle is captured, the data can be transferred to a terminal PC. There the acquired data can be visualized and analyzed.
To achieve a maximum flexibility regarding data rates the signal generation block for the measurement cycles, the ADC device and the PC interface are considered as running at different clock rates asynchronously. This splits the design in separate clock domains.

A high-speed 12 bit ADC was used to digitize the analogous output voltages of sensor chips. Simulations showed that the sampling noise of a 12 bit converter is sufficiently low to not impact the distance result. The memory size needed for one phase step is 20 bit for each pixel due to internal preprocessing. For a pixel array size of 128×128 of the camera, where 16 phase steps are acquired per pixel, one distance measurement frame leads to a memory demand of 5.24 Mbit.

Because of the demanded memory size, the requirement to flexibly generate all needed computation signals and to fetch the data with an adequate clock frequency an FPGA device has been chosen as central computation element. We selected the Terasic DE4 FPGA board, containing a Stratix IV FPGA from Altera. Many in-system memory blocks are provided within this device. Furthermore, a high-speed ADC can be easily interfaced since many serializer/deserializer-blocks (SERDES blocks) are implemented in this FPGA type. While the Stratix IV series is ideal for testing and characterizing the whole TOF measurement system it would be no choice for a consumer product. This FPGA type would be too expensive. Furthermore, for a commercial product it is not necessary to have the same flexibility as the system possesses presented within this work. The current system occupies 9% of the logic and 38% of the memory blocks of the EP4SGX230 device. Thus, enough resources are available for future enhancements. Timing constraints were checked by Altera’s TimeQuest tool.

A. Initiate a new measurement

Fig. 5 illustrates a simplified block diagram of the measurement system for a measurement cycle. All periphery components have to be initially configured before the first measurement cycle can start. This includes the oscillator that provides the clock for the signal generation block. This clock generator can either be an onboard SIS570 PLL oscillator that has a sufficient jitter performance for TOF measurements or an external clock generator. Moreover various parameters have to be programmed to the memory space of the FPGA used for configuration data. These parameters include the duration of the CALIB and RESET signals and the integration time length that can be set independently in a range from μs to ms. Moreover, the pixel array size can be chosen up to 128×128 elements. To meet the requirements for characterizing TOF pixels all measurement parameters can be varied in a very broad range.

Fig. 4 illustrates the simplified excitation sequence for a TOF measurement using the pixels from [5]. A new measurement cycle is started by setting the RESET and the CALIB signal sequentially. Afterwards the actual measurement, the correlation process of the electrical reference and the optical received signal, can be started. This is done by releasing the RESET and CALIB signal. Furthermore, both the reference and the modulation clock have to be applied to the camera chip and the illumination source, respectively. Most measurements are done with 16 equidistant phase steps with an incremental phase shift of 22.5°. This value was chosen because TOF systems suffer from an error of the measured distance. This error is dependent on the measured distance itself due to aliasing effects when sampling the ideal correlation triangle [6, 7]. It is negligible for 16 phase steps and increases with a decreasing number of phase steps. Furthermore a Fourier Transform is required for acquiring the phase shift of the correlation triangle. Thus a value of 16 phase steps is ideal since an FFT can be implemented very efficiently for 2^N samples.

Both the modulation and the reference clock are generated by two parallel-in serial-out shift registers with a length of 16 bits. While one shift register has always an initial data value of 0x0F the same initial data is set to the second shift register only for ϕ = 0°. When applying, e.g., ϕ = 22.5° or ϕ = 180° to the signal of the illumination source, the initial variable for the second shift register is 0x1E or 0xF0, respectively. The selected approach helps to implement the clock generators in an efficient way. The frequency of both clock signals can be varied between 10 to 20 MHz. For most measurements 16 equidistant phase steps ϕ are sufficient. Thus the maximum clock frequency of the shift registers is 320 MHz in this case. Although the internal PLL blocks of the FPGA are better suited for generating these clock signals, the PLLs can generate square wave signals only. Future improvements require issuing periodical serial data on the clock outputs.

During the integration time both, the reference- and the modulation clocks are integrated according to the correlation
A high optical power of the incident signal may result in a saturation of the TOF pixel. To prevent this effect a short integration time should be chosen. However, when the optical power of the incident signal is very low, the standard deviation of the measured distance will be high resulting in an imprecise distance measurement. It is possible to minimize the standard deviation by numerically averaging over a large number of measured distances. However, this will require many measurements and readout cycles and is therefore very time and resource consuming. A way to reduce this inefficient overhead is to extend the integration time since the pixel is unlikely to saturate at small optical power values of the incident signal. Therefore, the integration time can be varied in a broad range and dynamically at runtime. This helps acquiring information about the saturation behavior of the TOF pixels.

TOF measurement systems basically rely on the signal delay caused by the finite speed of light. To obtain a change of the measured distance of 1 cm the propagation delay of the optical signal changes with 66.7 ps. Hence TOF systems require a high time resolution to achieve a high distance resolution. The Stratix IV FPGA family suffers from a maximum total period jitter of 300 ps on their LVDS outputs [8]. To avoid any influence on the measured distance from this jitter all signals are reclocked by means of high-speed ECL logic. With this approach the RMS period jitter is reduced to 1 ps [9], making it negligible for characterizing the TOF pixels.

For the characterization of a single TOF pixel a laser is preferred. Here the light is guided through a single-mode fiber to the TOF pixel. No additional optical components like lenses are required that would have an impact on the characterization. Moreover the optical power can be adjusted precisely since the core of the fiber has a smaller diameter than the PIN photodiode of a TOF pixel. This ensures that all the optical power is received by the photodiode of the pixel. When background light should be emulated a second laser can be inserted in the optical path [5]. This shows that a fiber based setup is an ideal way to systematically characterize single TOF pixels. For characterizing a TOF pixel array, both, a laser or a LED light source can be used. When using a laser the distance from the end of the fiber to the chip has to be extended to illuminate the whole chip area. However, not all pixels will receive the same optical power since it will be distributed in a Gaussian shape over the area. In contrast to an LED light source no optical components are required here.

B. Read in of the output voltages

After the integration operation is completed, the read in of one point of the correlation triangle from the camera chip begins. Fig. 6 illustrates a simplified block diagram of the measurement system for this case. This task is started with the help of the SELECT signal. The integration process stops with the first rising edge of the SELECT signal in every single TOF pixel. Then one voltage of the correlation triangle of the first eight pixels is connected to the output buffers. With every following rising edge of the SELECT signal the next eight pixel voltages are issued at the output. To meet the speed of the output drivers of the camera chip, the SELECT signal has a frequency of 10 MHz.

The output signals of the camera chip are converted by an 8 channel ADC of which each channel possesses a resolution of 12 bits. The obtained data are transmitted as a serial stream to the FPGA after conversion. The conversion rate of the ADC was set to a fixed rate of 60 MSPS. This leads to a total data rate of 5.76 Gbps. Furthermore, the ADC clock is independent of the clocks of all other function blocks. This makes the ADC/FPGA interface reliable under all operation conditions of the camera system. A full data transfer for one point of the phase triangle takes a time of 1.64 ms in this system assuming the camera chip has a pixel array size of 128×128 and is read out with 10 MHz. During this time no measurement cycles can be executed by the camera chip. For a system that is designed for characterization the dead time due to the read out process is irrelevant. However, when a large frame rate has to be achieved, this transfer time must be minimized by, e.g., maximizing the number of output channels of the camera chip.

At the input of the FPGA the serial data streams are parallelized by the built-in LVDS-SERDES blocks. To suppress noise from interference on the analogous output voltages of the 3D camera chip, it is possible to average over a maximum of six sequential ADC samples. Afterwards the data is forwarded to the memory controller. This block is running at the clock frequency of the USB interface that is asynchronous to the clock of the ADC block.

To store the correlation triangle, the synchronous memory blocks of the Stratix IV device are used. This feature prevents the need for an external SRAM memory. The memory controller possesses two different write modes. The first mode is the write only mode. When new data is brought to the input of the block, the 12 bit wide data word is stored to the 20 bit wide memory cell. The upper 8 bits of the memory word are left blank. The memory address of the data word is derived from the pixel number and the obtained phase step. The second operation mode of the memory controller is the averaging mode. Here the new input data word is accumulated to the current value stored in the memory cell. However, an addition is preferred over a true averaging since this increases the resolution of the ADC virtually. This mode is necessary when the power of the optical signal is very low. Even for very long integration times the standard deviation of the measured distance is high [5]. By averaging over multiple correlation results the standard deviation can be reduced by $1/\sqrt{N}$ where $N$ is the averaging.
count. However, this leads to a decrease of the overall frame rate. Since one memory word is 8 bit wider than one ADC data word, it is possible to average over 256 triangles without the occurrence of an overflow assuming a maximum value input word.

C. Transfer to a terminal PC

Fig. 7 illustrates a simplified block diagram for the readout process. After a full correlation triangle with all demanded averaging cycles was stored to the SRAM memory, the measurement process is completed and the data is sent to the terminal PC via the USB interface using an FT2232H device working in FIFO mode. Therefore a simple state machine was implemented to the memory controller that shifts the data from the memory to the USB FIFO byte per byte. To provide a basic data integrity check, a checksum is attached to every data package. At the terminal PC the data is reassembled and transmitted to Matlab for analysis and visualization. Now a new measurement cycle can be started by the terminal PC.

IV. ENHANCED MEASUREMENT FEATURES

Thanks to the modular structure of the described characterization system many additional devices can be added to a measurement setup. The light source illustrated in Fig. 5 is connected via an SMA connector. This gives the freedom to insert optional devices like an arbitrary waveform generator into the signal path. This setup was used to emulate the limited bandwidth of an illumination source based on LEDs that is dependent on its temperature \cite{3,4}. Furthermore a PCB that is capable of generating a random cycle-to-cycle jitter with a Gaussian histogram shape can be inserted instead of the arbitrary waveform generator. This can be done to investigate the impact of jitter of the modulation clock on the distance measurement result. A discrete jitter can be expected when a signal with a high Gaussian cycle-to-cycle jitter is reclocked. To emulate this effect the flexibility of an FPGA is beneficial. A VHDL function block that modifies a signal with a discrete jitter can be simply inserted before the reference and modulation clock outputs. This example outlines that this characterization system can be easily reconfigured to include new features. Thus many additional parameters of TOF pixels can be investigated flexibly in short time.

V. MEASUREMENT SYSTEM

The measurement system built in our laboratory is depicted in Fig. 8a. The main device of the measurement system is a Terasic DE4 board which is based on a Stratix IV FPGA device. The FPGA can communicate with a terminal PC via a USB FIFO that is attached to the board on the right.

The camera chip is inserted on a separate board. This PCB is connected via Altera’s high-speed mezzanine card interface (HSMC-interface) to the FPGA board. Over this interface all signals are routed. Furthermore, the board is powered over the HSMC bus. The board possesses clock generators as well as all needed devices to relock the control signals, e.g., the modulation and reference clock, the RESET and the CALIB signals, as well as others. The illumination source, in this case a single-mode laser, can be attached via the SMA connectors on the very left side of the board. As can be seen in Fig. 8b the system is used to characterize a single TOF pixel. This is done by means of an optical fiber. After the integration process is completed the camera chip is read out with the help of an ADC. Then the data is transmitted via the HSMC-interface to the FPGA and after pre-processing to the terminal PC.

VI. RESULTS

To the best knowledge of the author, no publication exits describing a dedicated TOF characterization system in detail. However, other publications \cite{7,11,12} use commercial products for determining properties of the TOF system. This approach minimizes flexibility and thus the ability to measure individual error sources independently. However, the advantage of their system lies within the costs.

In Publication \cite{5} the dependence of a TOF pixel on the background light is investigated. At high intensities of background light the integration time \(T_{int}\) has to be chosen very short since the pixel circuitry tends to saturate. However, at short \(T_{int}\) the standard deviation \(\sigma\) of the measured distance

\[
\sigma = \frac{\text{height of the histogram}}{\text{distance measurement}}
\]
increases. Furthermore, in case of a very weak received optical signal $P_{\text{opt}}$, $\sigma$ can be high for long $T_{\text{int}}$ as well. In this case the mentioned averaging function can be applied. This increases the integration time virtually. The standard deviation decreases by $1/\sqrt{N}$ with $N$ as number of the averaging cycles. The averaging process is solely done by the FPGA. Thus the USB interface is relieved and the PC load consequently decreases. Due to the ECL reclock circuitry used in the system the random cycle-to-cycle jitter could be reduced to 1 ps. This corresponds to a measured distance standard deviation of 0.15 mm. Using this system in combination with the pixel from [5] a $\sigma$ of 1 cm could be achieved for one correlation triangle, i.e., a $T_{\text{int}}$ of 140 $\mu$s and a $P_{\text{opt}}$ of 10 nW (Fig. 9). For Fig. 10 the averaging function was enabled with 256 elements. Here the parameter range of a minimal $\sigma$ increases dramatically. Furthermore, the standard deviation of the distance can be reduced to 2 mm. No background light was applied during the measurements. In comparison, the standard deviation amounts to a total of 30 mm at D-Imager of Panasonic [10] without any background light. The standard deviation of our pixel, investigated with the presented measurement setup, is smaller by a factor of 15.

VII. CONCLUSION

In this paper we presented a powerful FPGA based characterization system for our TOF 3D camera chips supporting a pixel count up to 128 $\times$ 128 pixels. Our measurements showed that a distance resolution down to 2 mm is achievable in a very broad range using the pixel presented in [5] with enabled averaging. To systematically investigate the capabilities of the TOF pixels the hereby reported system can flexibly change the length of all generated control signals in a broad range from several $\mu$s to hundreds of ms. Moreover, all control signals possess a minimal jitter of 1 ps to meet the required time resolution. Transposed into the TOF approach, the thereby introduced measurement error amounts to only 0.15 mm. After the system acquires the distance information from the TOF chip, it can average over a maximum of 256 correlation triangles. Being done independently from the terminal PC, this feature increases the integration time virtually and is important for improving the standard deviation. Thanks to the modular structure of the system, additional devices for parameter characterization can be integrated easily.

REFERENCES